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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,853	01/31/2001	Tony San	ALTRP054/A574	3570
51501	7590	07/12/2005	EXAMINER	
BEYER WEAVER & THOMAS, LLP ATTN: ALTERA P.O. BOX 70250 OAKLAND, CA 94612-0250			STEVENS, THOMAS H	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/773,853

Applicant(s)

SAN ET AL.

Examiner

Thomas H. Stevens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-44 were examined.

Section I: Response to Applicants' Arguments (1st Office Action)

35 USC § 102/103

2. Applicants are thanked for addressing this issue. Applicants state neither prior art rejection states a filter resource estimator. Examiner refutes this argument based on the specification's vague definition of what a filter resource estimator does (specification: pg. 5, lines 10-15). Rejection stands.

Section II: Non-Final Rejection (2nd Office Action)

Oath/Declaration

1. The oath or declaration is defective. The oath or declaration is defective because: provisional application number 60/186,575 is not listed. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application-by-application number and filing date is required. See MPEP §§ 602.01 and 602.02.

Claim Objections

1. Claims 2-6 are objected to since the preamble of the independent claim recites a filter compiler while claims 2-6 recite compiler.
2. Claims 17-20 are objected to since claims 17-20 state a compiler as recited in claim 16 that does not exist.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

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The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement and enablement requirement.

The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification merely mentions a filter resource estimator without definition.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 recites the limitation of "filter" (line 7) while the preceding lines state various types of filters (i.e., filter coefficient; filter resource; filter compiler). There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed

in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-7,11,12,14-22,26,37-40** are rejected under 35 U.S.C. 102(e) as being disclosed by **Dick et al** (U.S. Patent Number 6.600.788), herein referred to as **Dick**.
2. As to **Claims 1 and 16**, **Dick** teaches a filter coefficient generator (**column 3, lines 42-45**), a filter spectral response simulator (**column 4, lines 8-12**), a filter resource estimator (**column 7, lines 51-57**) and a filter compiler unit (**column 5, line 64-column 6, line17**). As to comparing the desired filter spectral response to the expected filter spectral response, **Dick** teaches implementing the equations that define the transfer function of the filter into a mathematical modeling environment and performing simulations until the design of the filter produces the desired results (**column 7, lines 23-30**). These simulations involve comparing the desired filter spectral response to the expected filter spectral response.
3. As to **Claims 2 and 17**, **Dick** teaches performing simulations of the filter until a design that satisfies a specific problem is determined experimentally (**column 7, lines 23-30**). It is determined that during simulation, filter parameters, such as coefficients, are tweaked until the filter is operating as desired, starting with a set of initial (first set) coefficients. When the simulated spectral response of the filter is substantially the same as what is desired or expected, the coefficients of the simulated model become the coefficients of the filter (or second set) that is to be implemented in the design.

4. As to **Claims 3 and 18**, Dick teaches estimating the implementation cost of the filter (**column 7, lines 51-57**). Estimating the implementation cost of the filter is done after the design of the filter (**Figure 1, element 13**) is finalized, therefore the second set of filter coefficients would be used.

5. As to **Claims 4 and 19**, Dick teaches a finite impulse response (FIR) filter (**Figure 2**).

6. As to **Claims 5 and 20**, Dick teaches the filter coefficients are FIR filter coefficients (**Figure 2, elements a_0 - a_3**), wherein the filter spectral response is an FIR filter spectral response (**column 4, lines 8-12**), wherein the desired filter implementation output file is an FIR filter implementation output file (**column 5, line 64-column 6, line 7**).

7. As to **Claims 6 and 21**, Dick teaches an FIR filter hardware implementation file provides a routing and placing dataset suitable for fitting the FIR filter in a programmable logic device (**column 5, line 64-column 6, line 17**), and a filter simulation file (**column 7, lines 23-30**).

8. As to **Claims 7, 11 and 22**, Dick teaches a modulator that re-quantizes input data samples from a high degree of precision to a lower degree of precision thereby reducing the number of resources required to implement the FIR filter in the FPGA (**column 2, lines 26-32**). It is concluded that a conversion from a floating-point coefficient to a fixed-point coefficient would be a change from a high degree of precision to a low degree of precision. Further, it is concluded that scaling and rounding the floating-point values to form the first set of filter

coefficient values would also be a change from a higher degree of precision to a lower degree of precision as taught by **Dick**.

9. As to **Claims 12 and 26**, **Dick** teaches that the equations that define the transfer function of the filter should be implemented in a mathematical modeling environment such as Matlab (**column 7, lines 23-28**). It is concluded that the Matlab modeling environment would utilize a Matlab Simulink or Testbench model.

10. As to **Claims 14 and 15**, **Dick** teaches the FIR filter fitted in a programmable integrated circuit such as a programmable logic device (**column 2, lines 20-21**).

11. As to **Claim 37**, **Dick** teaches a method of building a decimating filter by a compiler using a plurality of domain polyphases (**column 8, lines 6-11**), each of the plurality of polyphases is represented by a serial filter (**Figure 6**), a single clock domain is used for each serial filter, a first clock rule when an input data width is less than or equal to a decimation factor (**column 8, lines 11-14**), a second clock rule when an input data with is greater than the decimation factor (**column 8, lines 38-41**).

12. As to **Claim 38**, **Dick** teaches setting a clock rate to an input data rate, and setting an output data rate equal to the input data rate divided by the decimation factor (**column 7, lines 11-14**). Further **Dick** teaches that the input sample is processed in a time-multiplexed manner (**column 8, lines 9-11**),

encompassing holding the input data for a number N clock cycles where N is equal to the decimation factor.

13. As to **Claim 39**, **Dick** teaches setting the clock rate equal to a first speed multiplication factor multiplied by the input data rate (**column 8, lines 38-41**). It follows from this that the output data rate would then be equal to the multiplication factor times the input data rate divided by the decimation factor as taught (**column 8, lines 11-14**). Further, **Dick** teaches that the input sample is processed in a time-multiplexed manner (**column 8, lines 9-11**), encompassing holding the input data for a number L clock cycles where L is equal to the first speed multiplication factor times the decimation factor.

14. As to **Claim 40**, **Dick** teaches the decimating FIR filter includes a final adder (**column 8, lines 19-21**).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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Patentability shall not be negated by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. **Claims 8-10, 23-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dick**, as applied to **Claims 1,16 and 22** above, and further in view of Shung et al (Shung et al, "An Integrated CAD System for Algorithm-Specific IC Design", IEEE Transactions on Computer Aided Design, Vol. 10, No. 4, April 1991), herein referred to as **Shung**.

18. As to **Claim 8-10, 23-25**, **Dick** teaches implementing equations of the FIR filter design in a mathematical modeling environment and performing simulations until the desired design result is attained (**column 7, lines 23-30**). Further, **Dick** teaches a modulator that re-quantizes input data samples from a high degree of precision to a lower degree of precision thereby reducing the number of resources required to implement the FIR filter in the FPGA (**column 2, lines 26-**

32). It is concluded that scaling and rounding the floating-point values to form the first set of filter coefficient values would also be a change from a higher degree of precision to a lower degree of precision as taught by **Dick**.

19. **Dick** does not explicitly teach this simulation environment including an input parameter buffer to store a plurality of FIR filter input parameters suitable for implementing the filter, the filter input parameters including a tap quantity value, a pipeline delay value, a parallel FIR filter architecture value, a serial FIR filter architecture value, and input bandwidth value and an initial set of FIR filter component values.

20. **Shung** teaches a CAD system used for the design of a FIR filter (**page 460, section 5.3, first bullet**) including an input parameter buffer to store a plurality of FIR filter input parameters (**page 452, section 4.1, sentence 4**), wherein the user specifies the target architecture as serial or parallel which encompasses a parallel and serial FIR filter architecture value (**page 448, section 2.2.1, first sentence**), the data paths which encompass a tap quantity value and pipeline delay value (**page 448, section 2,1,2, second paragraph, first sentence**), and filter parameters which encompass an input bandwidth value and an initial set of FIR filter coefficient values (**page 448, section 2,1,1, sentences 2 and 3**).

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21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the simulation environment as taught in **Shung** as the mathematical modeling environment as disclosed in **Dick** since the environment as taught in **Shung** allows the user to define the target architecture (**page 448, section 2.2.1, first sentence**), the data paths (**page 448, section 2,1,2, second paragraph, first sentence**), and filter parameters (**page 448, section 2,1,1, sentences 2 and 3**).

22. **Claims 13, 27-29, 41-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dick** as applied to **Claims 1,5,16 and 21** above, and further in view of Saramaki et al (Saramaki et al, "Design of Computationally Efficient Interpolated FIR Filters, IEEE Transactions on Circuits and Systems, Vol. 35, No. 1, January 1998), herein referred to as **Saramaki**.

23. As to **Claims 13 and 27-29**, **Dick** teaches a polyphase or multi-rate configuration, such as a decimator (**column 8, lines 6-8**). Further, **Dick** teaches the FIR filter fitted in a programmable integrated circuit such as a programmable logic device (**column 2, lines 20-21**).

24. **Dick** does not explicitly teach a multi-rate filter such as an interpolating FIR filter.

25. **Saramaki** teaches interpolating FIR filters and decimation as two approaches to decreasing the required filter length (**page 70, second column, last paragraph**).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interpolating FIR filter as taught in **Saramaki** as an alternative to a decimating FIR filter as taught in **Dick** since interpolating FIR filters and decimation filters both reduce the length of filters as taught in **Saramaki (page 70, second column, last paragraph)**.

27. As to **Claim 41**, **Dick** teaches building an FIR filter using a plurality of domain polyphases wherein each of the plurality of polyphases is represented by a serial FIR filter (**column 8, lines 6-8**).

28. **Dick** does not expressly teach the FIR filter being an interpolating FIR filter and using the interpolation factor for a first and second clock rule.

29. **Saramaki** teaches an interpolating FIR filter as a cascade of FIR filters (**page 70, equation 2 and description**) where the interpolation factor, L , determines how many stages or multipliers a design has (**page 71, paragraph 1**). Further, **Saramaki** teaches interpolating FIR filters and decimation as two approaches to decreasing the required filter length (**page 70, second column, last paragraph**).

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interpolating FIR filter as taught in **Saramaki** as an alternative to a decimating FIR filter as taught in **Dick** since interpolating FIR filters and decimation filters both reduce the length of filters as taught in **Saramaki (page 70, second column, last paragraph)**. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the interpolation factor, as taught in **Saramaki** to modify the clock rules for an interpolation filter as taught in **Dick** since the interpolation factor determines how many stages a design would have as taught in **Saramaki**, making the interpolation factor similar to the decimation factor.

31. As to **Claim 42**, **Dick** teaches setting a clock rate to an input data rate, and setting an output data rate equal to the input data rate divided by the interpolation factor (**column 7, lines 11-14**) wherein the interpolation factor determines how many stages are included in the filter (**see paragraph 45**). Further **Dick** teaches that the input sample is processed in a time-multiplexed manner (**column 8, lines 9-11**), encompassing holding the input data for a number P clock cycles where P is equal to the interpolation factor.

32. As to **Claim 43**, **Dick** teaches setting the clock rate equal to a second speed multiplication factor multiplied by the input data rate (**column 8, lines 38-41**). It follows from this that the output data rate would then be equal to the

multiplication factor times the input data rate divided by the interpolation factor as taught (**column 8, lines 11-14**) wherein the interpolation factor determines how many stages are included in the filter (**see paragraph 45**). Further **Dick** teaches that the input sample is processed in a time-multiplexed manner (**column 8, lines 9-11**), encompassing holding the input data for a number R clock cycles where R is equal to the first speed multiplication factor times the interpolation factor.

33. As to **Claim 44**, **Dick** teaches the interpolating FIR filter includes a state machine that controls a select bus coupled to a final multiplexer (**Figure 6, element 61**).

34. **Claims 30-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dick** as applied to **Claims 16 and 21** above, and further in view of Mintzer (Mintzer, Les "Digital Filtering in FPGAs", **Conference Record of the Twenty-Eighth Asilomar Conference on Signals, Systems and Computers**, Vol.2, pages 1373-1377, 1994), herein referred to as **Mintzer**.

35. As to **Claims 30, 34 and 36** **Dick** teaches estimating the implementation cost of the filter by determining the filter type by showing examples of cost analysis done for different filters (**column 7, line 54 and column 10, line 28**), a serial filter type (**Figure 6**), finding a size of a serial tap delay line (**column 7,**

lines 20-30), dividing the second set of filter coefficients into a number N of groups (**column 6, lines 34-44**), evaluating a number of logic elements required to implement the FIR filter (**column 7, line 54**), wherein the estimate is a number of logic cells required to implement the FIR filter (**column 7, lines 62-67**).

36. As to **Claims 31,32,33, and 35**, **Dick** teaches a parallel filter type (**Figure 8**), finding size of a parallel tap delay line (**column 7, lines 20-30 and lines 45-48**), dividing the second set of filter coefficients into a number of groups (**column 6, lines 34-44**), finding a size of a ROM LUT for a plurality of partial products (**column 7, lines 49-57, (MUL) and lines 62-63**), and finding a size of an adder tree for the plurality of partial products (**column 7, lines 49-57, $\Gamma(\text{ADD}_z^{-1})$**), calculating filter resource estimate wherein the parallel filter resource estimate is a number of logic cells required to implement the parallel filter (**column 7, lines 54, 62-67**). It is noted that this step would be repeated for additional groups if necessary.

37. **Dick** does not expressly teach determining a filter symmetry.

38. **Mintzer** teaches that exploiting symmetry realizes a significant hardware reduction (**page 1376, column 1, 3rd paragraph**).

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include filter symmetry as taught in **Mintzer** in the cost estimation as taught in **Dick** since symmetry allows a significant hardware reduction as taught in **Mintzer** (**page 1376, column 1, 3rd paragraph**).

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Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571) 272-3749. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

June 28, 2005

THS

 7/8/05
Paul L. Rodriguez
Primary Examiner
Art Unit 2125